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LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS
(Continued)

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SECTION 1

INTRODUCTION

The following is [redacted] 25X1 response to Item B of the five technical items which were asked to be investigated on the 105 Program. Items C, D and E have been investigated and a technical proposal has been submitted on 26 March 1965.

Item B is the study of what will be required to incorporate the silicon diode array data block in place of the FONT-Hammer approach. After a careful investigation it has been determined that, using the silicon diode array, there was only one possible method that can be proposed at the present state of the art. This method produces 56 alpha-numeric characters with the addition of a 280, eight bit machine code added storage inside the same data block area. Fourteen (14) of these 280, eight bit machine codes will be used as index marks so that effectively there will be 266 eight bit words of storage. This method will be described in Section 2 of this report. If it is required to produce only 128 machine characters, this same chip construction would be used and only 128 cells would be wired up. The cost difference would be very slight between the two systems.

In order to incorporate the silicon diode array data block in place of the FONT-Hammer approach it will be required that the data block information be stored in some type of storage device so that, if multiple chip copies are required, a permanent record will be available. In addition to the required storage there must be a Decode-Encode type of logic required to convert the American Standard Code into an alpha-numeric character to be printed. These two functions will require the majority of the added space required.

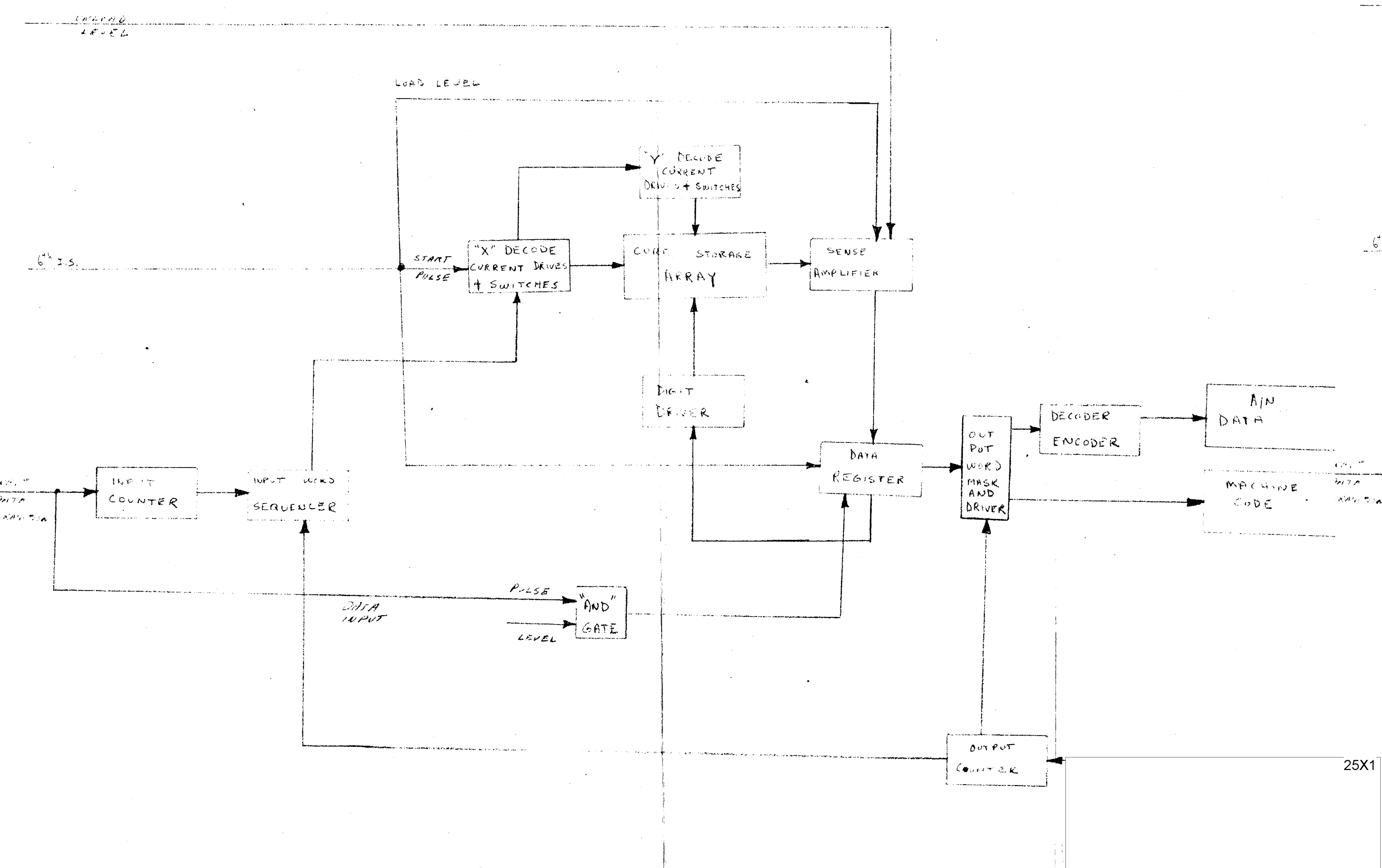
Included in this report are the costs, the additional space and power supplies required to incorporate this change into the presently conceived "Chip Printer Unit".

SECTION 2

ALPHA-NUMERIC WITH EXTRA DATA STORAGE

As can be seen in Figure 1, the input information will be supplied from the input station as was described in the Final Study Report of the chip printer unit. This system was such that when the proper Item Separator has been read in, the data required by the data block readout circuit will be presented to the core storage unit. The "load level" signal will also be provided to the core unit at the same time that the input data is presented to the memory unit. The input data will be presented to the pulse side of an "AND" gate. From there it will be given to the input data register. In order to supply the data in the proper sequence an input counter with an input word sequencer is provided. The data is stored in the core array in such a fashion that when it is removed, it will be removed with one alpha-numeric character and five machine storage character codes per cycle. The data register will place the alpha-numeric character code into the first storage of memory as given by the X and Y location counters. This information will also be placed into the 57th memory location. The input word sequencer will place a machine code representation of the alpha-numeric in location 2 and also its machine code representation in location 58. In this way the core memory will be loaded with alpha-numeric characters starting at location 1 and going up to 56 locations. The machine code will start at 57 and go all the way to 338.

In order to accomplish this, a standard memory unit of 512, 8 bit words will be required. The added memory could be used for any future growth that might require additional memory.



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DATA RECORDING CONTROLS
FIGURE 1

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The next smallest standard memory unit size available is a 256 word unit which is not adequate to meet our requirements. When the entire input information has been completely read into the core memory, the load level signal will be removed and the core storage unit is now ready to supply the output information to the silicon light pulser array.

At the appropriate time in the chip printer cycle, an unload signal will be given to core storage which will allow the first cell location and the 58th cell location to appear at the output data register. This information will be presented such that five words of machine code will be presented to every new alpha-numeric word that is presented. A full description of why this 5:1 cycle rate will be found in a detailed description which follows in Section A. 1. When the second alpha-numeric character is presented to the output circuit, the sixth machine code will be also presented at the output circuit. The alpha-numeric is made up of a 6 x 5 diode array, and rather than waste all of the machine code space beneath the letter, they are filled up in sequence by machine characters such that five machine codes will fit into the place of one alpha-numeric representation. As each alpha-numeric and machine code is written out to the data output register, the read-write cycle is such that the words are placed back into memory in their former location. This would mean that if more than one chip is required, this information will be present in the same locations in memory.

The memory unit will have incorporated in it all of the circuitry required to load and unload memory in the proper fashion and also to supply input-output buffer levels. Figure 2 shows the added electronic racks that will be required to perform this function.

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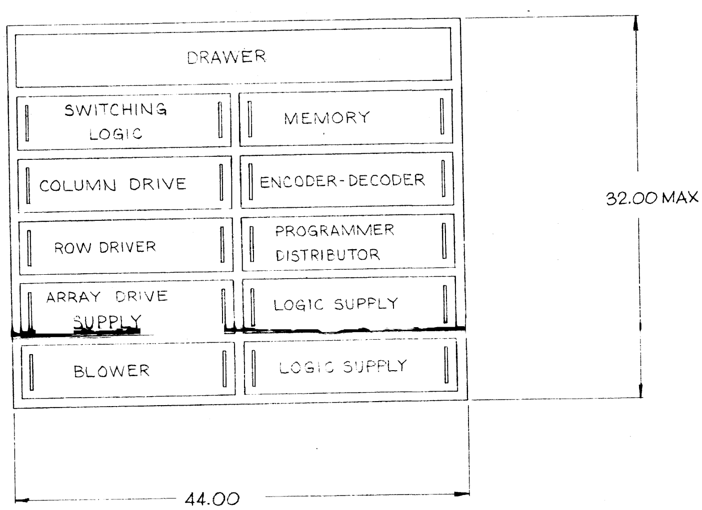

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GENERAL MANUFACTURING INSTRUCTIONS SPI 4.0 ARE PART OF THIS DRAWING.
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TOLERANCES: TWO PLACE DEC ± .02, THREE PLACE DEC ± .005, ANGULAR DIM. ± 1°0'

MATERIAL:

FINISH:

DR ____ DATE ____
CHK ____ DATE ____
ENG ____ DATE ____
MATLS ____ DATE ____
MFG ____ DATE ____
STDS ____ DATE ____
REL ____ DATE ____
CH DR ____ DATE ____
APPD ____ DATE ____
APPD ____ DATE ____

DWG TITLE FIGURE 2
ADDED CABINET SPACE REQUIRED

CODE IDENT NO.	SIZE	DRAWING NUMBER
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SCALE | WT ACT. | CALC | LB | SHEET | OF

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

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LARGE FORMAT - 280 "8" BIT WORDS

A. 1 TECHNIQUE OF DATA RECORDING

The method of accomplishing the recording of alphabetic and numeric characters and digital data on the film chip uses a unique method which [redacted] has recently developed. 25X1

It offers a more uniform universal type of character generation and allows many more time the machine code information to be stored onto the chip data block.

This method employs a matrix of silicon diodes operated as light generators. The array of silicon light pulser diodes is a proprietary device of [redacted] 25X1

[redacted] 25X1

A complementary product line developed using the same manufacturing techniques consists of linear arrays of photodiodes. These devices are used in automatic data readers. Reader design if simplified by an order of magnitude over present designs when recording is performed by an SLP array and reading by a corresponding photodiode array. The reason is the extreme dimensional accuracy of every bit position in both arrays. As a result, significant cost savings can be expected for the automatic reader.

A. 1. 1 Silicon Light Pulser

The Silicon Light Pulser consists of a silicon planar p-n junction which has two output terminals designated the anode and cathode. The device exhibits a voltage/current characteristic similar to that of a standard silicon diode, (see Figure A1). The diode has a high conductance forward voltage region, a low conductance reverse voltage region and a high conductance avalanche region.

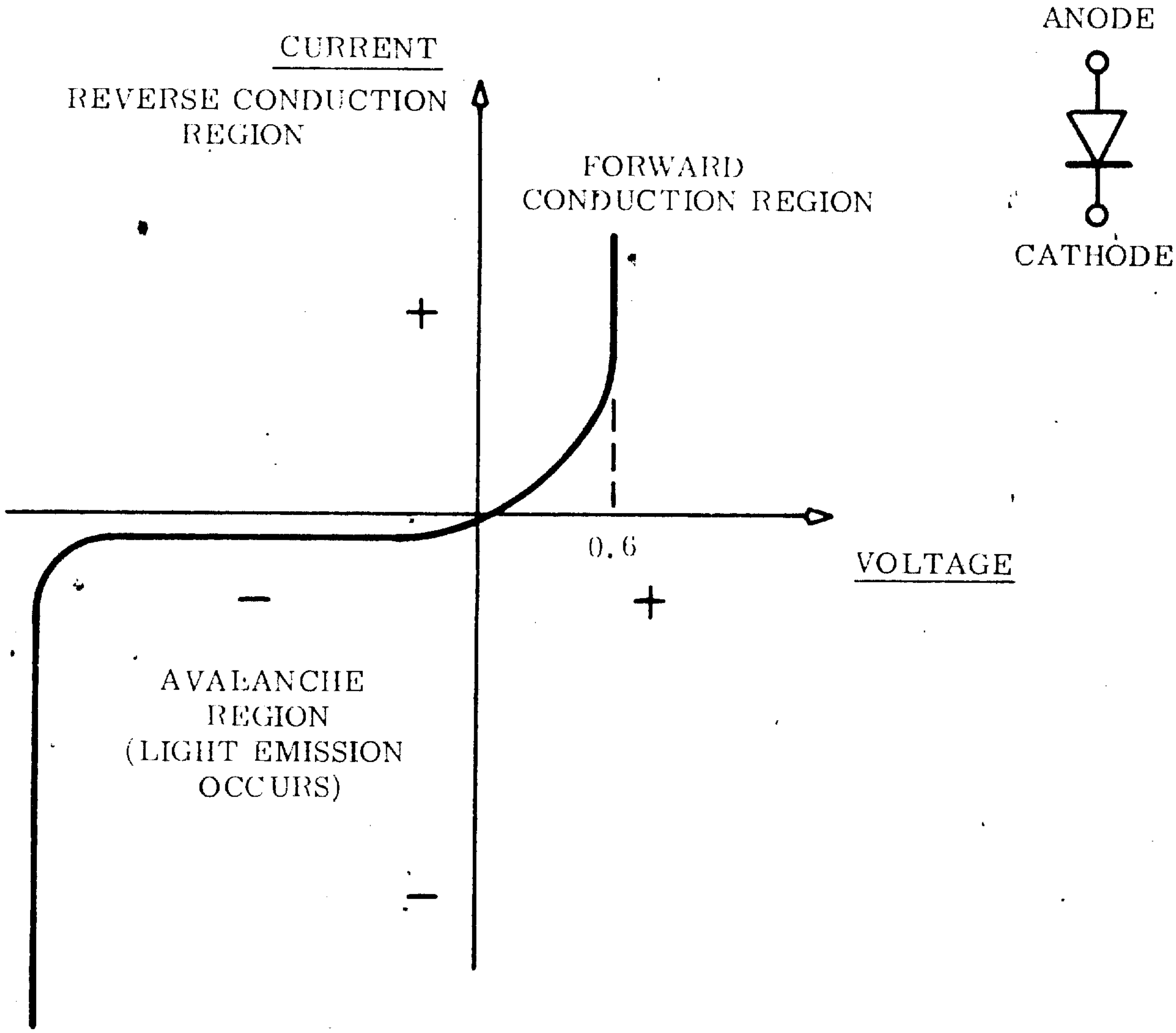

FIGURE - -1. TYPICAL SILICON DIODE CHARACTERISTIC

Normal diodes are usually operated in the two former regions while the Silicon Light Pulser operates in the latter.

When the reverse voltage is raised beyond the avalanche threshold, the diode conducts heavily and a visible light is detected around the region of the junction, (see Figure A2). The fundamental mechanism considered responsible for the emission of light from the avalanching junction is radiative transitions of "hot" charge carriers crossing the junction under the influence of the intense electric field on the order of 10^6 volts per centimeter existing in the depletion layer of the avalanching junction. These hot carriers have a broad distribution of energy and, therefore, the spectral distribution of the photons emitted on recombination is fairly broad. If transitions occur deep in the bulk of the silicon most of the shortwave length photons are absorbed by the silicon and the emitted light peaks sharply in the red and infrared portions of the spectrum. However, by designing a structure which forces the avalanche breakdown to occur close to the silicon surface, an appreciable amount of light can be generated in the blue-green region of the spectrum and the emitted light will appear as a warm white to the eye. In the optimized structure developed for the photographic recording application, the spectral distribution of the emitted light over the visible region approximates the radiation from a black body having a color temperature of 2500°.

Microscopically, the light source appears as a line source having a brightness at maximum usable current density levels estimated to be in the range of 5,000 ft.-lamberts. However, this high brightness value must not be confused with a high total light output because the emitting area is extremely small. The light is emitted from a line source and in the matrix array, this line source is actually 6 mils in length and 0.3 microns wide.

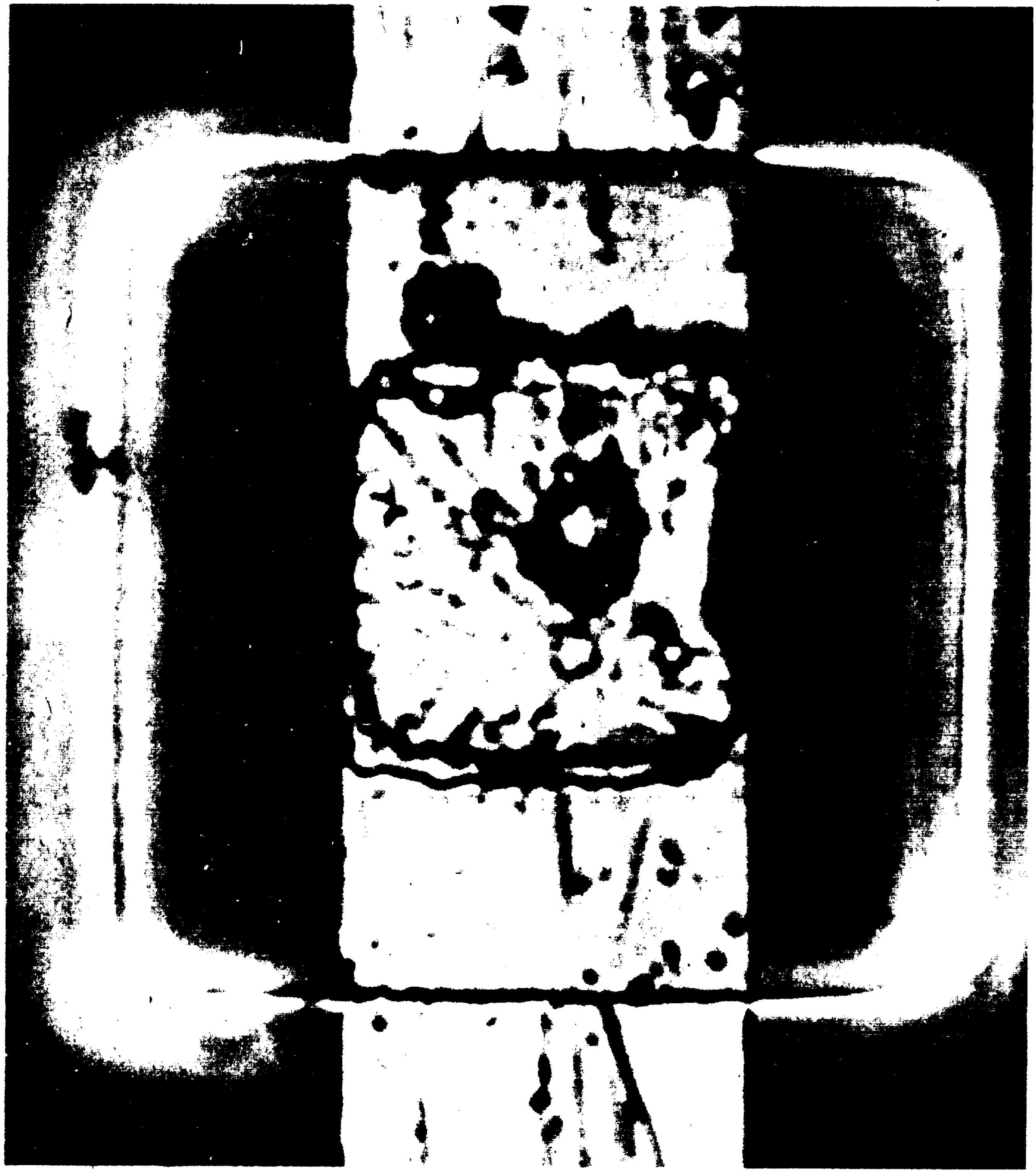

FIGURE A-2. SILICON JUNCTION EMITTING AVALANCHE LIGHT

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In the film recording of digital data, it is desirable that the data bit be recorded as a round dot having a density profile 4.5 mils in diameter at the 50% transmission point. Because the light is emitted from essentially a line source, a means of producing a round, uniformly dense dot of finite area from this source must be devised. The problem is solved by spacing a photographic emulsion at the proper distance from the source and shaping the source to approximate a circle so that the lambertian distribution of light from each point in the source combines at the emulsion plane of the recording material to provide the desired density profile. Figure A-3 illustrates a series of constant illuminance contours for two spatially separated point sources, indicating how the desired density profile is achieved by spacing the recording emulsion at a given distance from the light source.

A recording light source matrix consists of diffusion isolated p-n junctions, (as shown in Figure A-4), fabricated in silicon by the Planar technology and interconnected by standard metal-over-oxide techniques. A single light pulser is energized by making electrical connections to the appropriate row and column of the matrix array. Crossover of the interconnecting busses is accomplished by using the oxide-protected isolation diffusions as the interconnections between the metalized row interconnect bars shown in the figure.

A.2 RECORDING HEAD

A.2.1 Format

The format area for recording information on film is 0.553 by 4.606 inches and is illustrated in Figure A-5. SLP diodes interconnected to form a matrix will record the various types of data on film as combinations of dots. The top row of the format will

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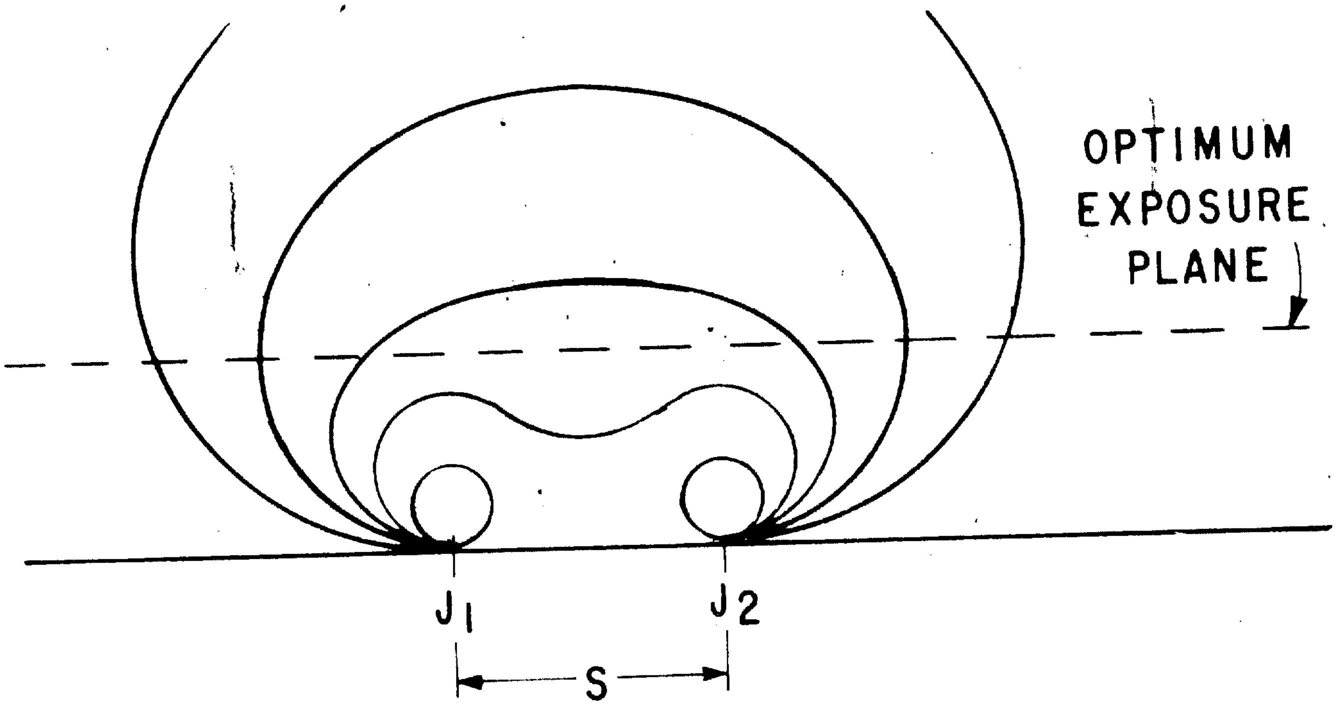

FIGURE A-3. CONTOURS OF CONSTANT ILLUMINATION FOR PARALLEL RECEIVER

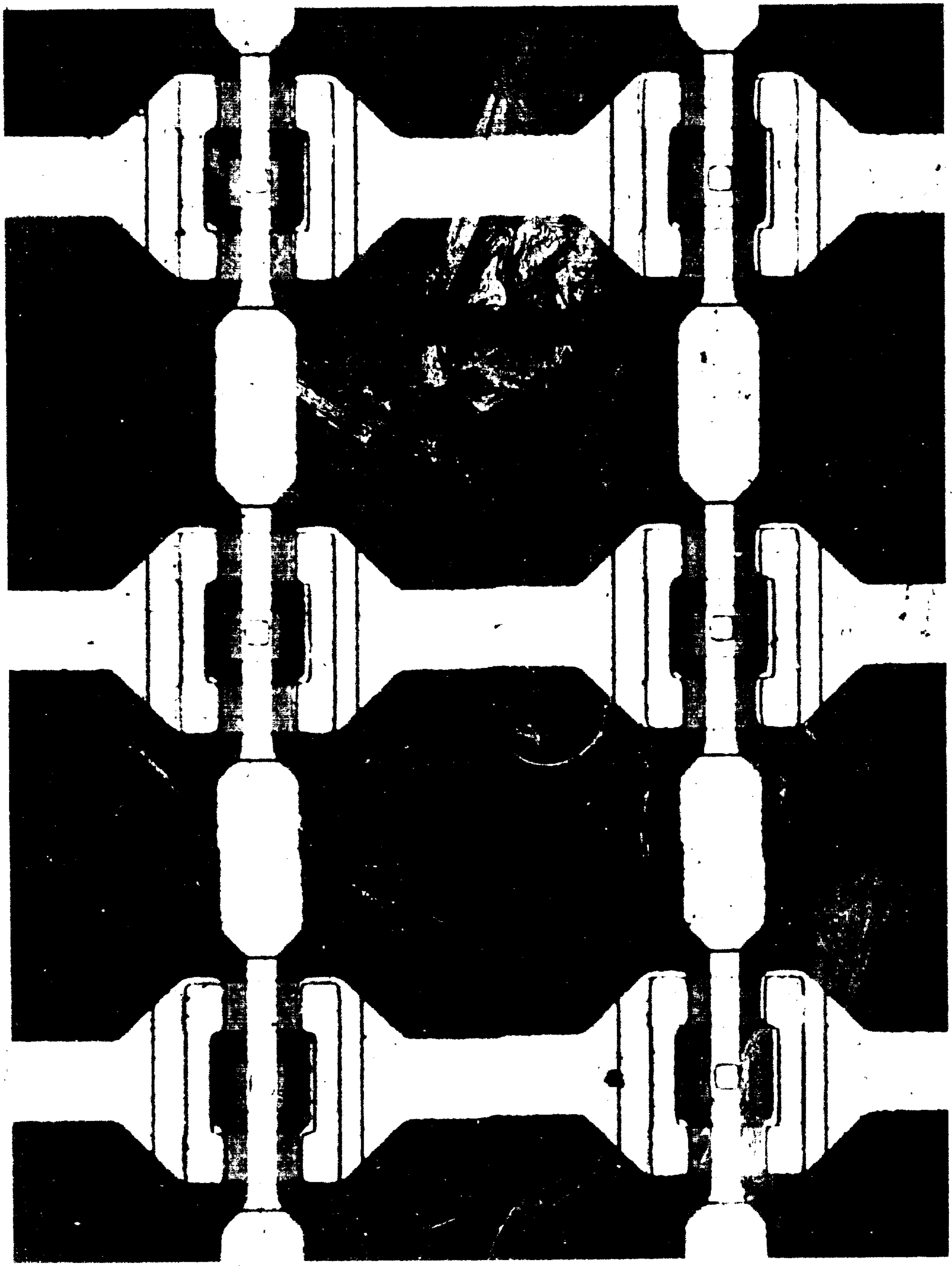

FIGURE [illegible]-4. SILICON LIGHT SOURCE ARRAY STRUCTURE

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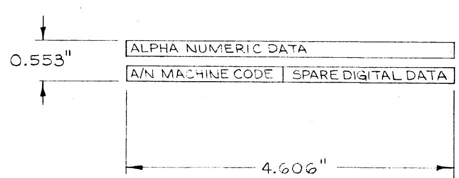

DRAWING NUMBER

25X1

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TOLERANCES: TWO PLACE DEC ± .02, THREE PLACE DEC ± .005, ANGULAR DIM. ± 1°0'

MATERIAL:

FINISH:

DR ______ DATE ______
CHK ______ DATE ______
ENG ______ DATE ______
MATLS ______ DATE ______
MFG ______ DATE ______
STDS ______ DATE ______
REL ______ DATE ______
CH DR ______ DATE ______
APPD ______ DATE
APPD ______ DATE

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DWG TITLE

FIGURE A-5
DATA FORMAT

CODE IDENT NO.	SIZE	DRAWING NUMBER
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SCALE	WT ACT. CALC LB	SHEET OF

be capable of displaying 56 alphanumeric characters. The remainder of the format will display digital data consisting of 266 eight bit binary words or 2048 binary bits. Adequate provision is allowed for index columns and rows to insure easy automatic readout of the digital data.

A portion of the digital data to be displayed will be the digital code corresponding to the alphanumeric characters.

The total information content of the display is dependent upon the SLP device pitch which is 0.009 inches. Experimental data to demonstrate the feasibility of this data packing is illustrated in Figure A-6 by a microdensitometer tracing of an experimental recording. The half amplitude dot diameter is 0.0045 inches and interference between adjacent bits would not be present. The substantial bit peak to background density difference should simplify the readout. The recording was achieved on SO-243 (ASA rating 1.6), when developed to a gamma of 2.3. The exposure consisted of an SLP current of 130 milliamperes and a duration of 6 milliseconds. The optical spacing between the film emulsion and the record surface was 0.002 inches.

A.2.2 Alphanumeric

To form each alphanumeric character it is intended to utilize the SLP diodes in a matrix type display. The area of the display is divided into equal size sub-zones. An SLP diode is placed in the center of each zone. If a character were superimposed on the display, some of the sub-zones would be covered by the line forming the character and some would not. To create this character with the matrix, those diodes corresponding to the sub-zones covered are energized. The line describing the character is, therefore, replaced by a series of dots.

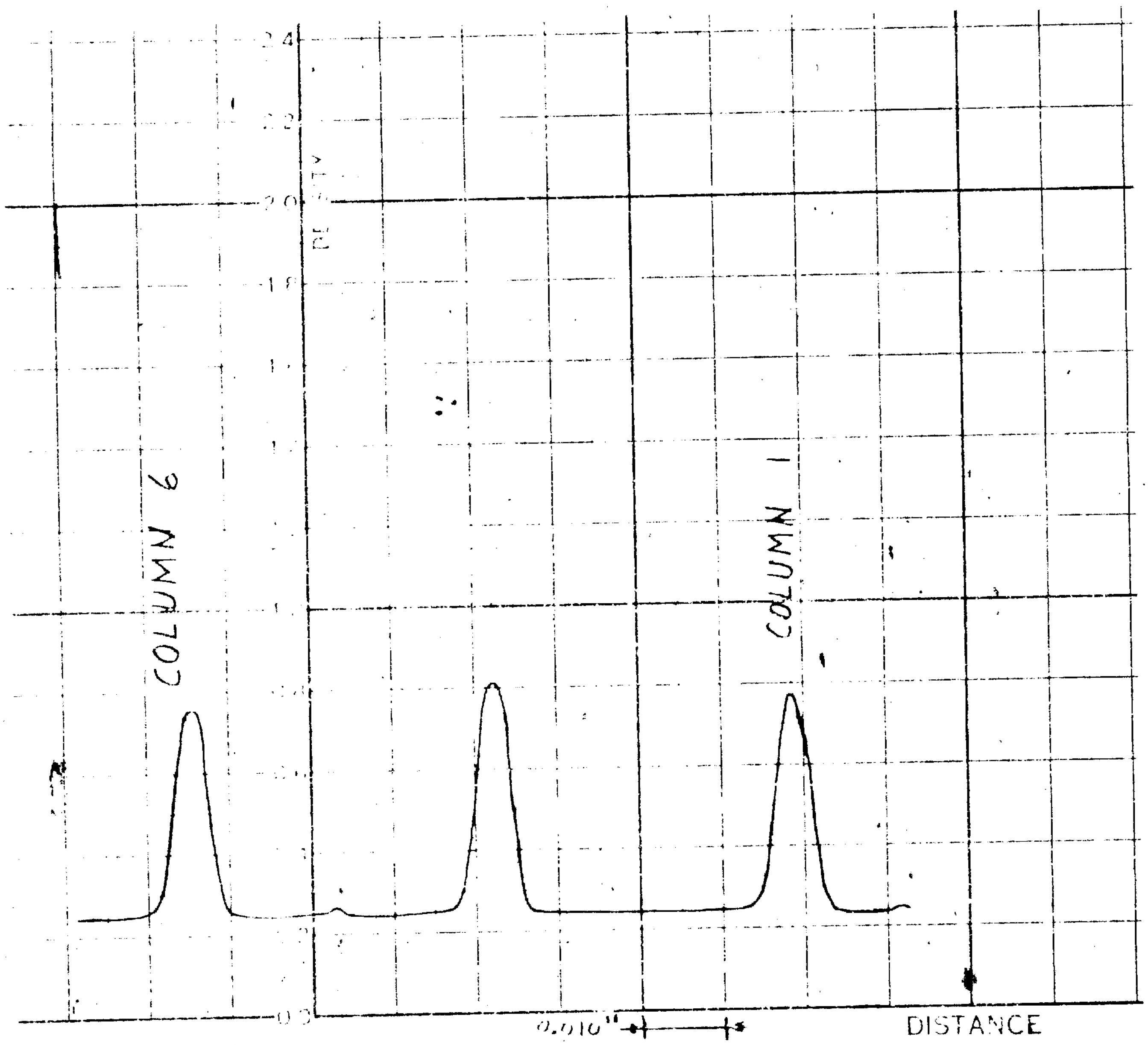

FIGURE A-6 MICRODENSITOMETER TRACE
EXPOSURE ON ASA 1.6 FILM

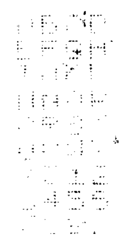

FIGURE A-7. ALPHA/NUMERIC CHARACTERS
5X6 MATRIX .0 18 INCH PITCH

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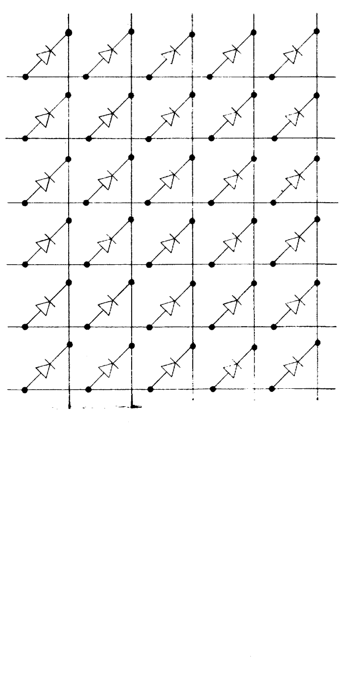
COLUMN

ROW



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APPD ____ DATE

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DWG TITLE FIGURE A-8
5x6 MATRIX SILICON LIGHT PULSERS

CODE IDENT NO.	SIZE	DRAWING NUMBER
72314	C	

SCALE | WT ACT. | CALC | LB | SHEET | OF

FCI-18-171 (10-64)
DEFIANCE NO. 1050

Figure A-7 is a sample of some characters created by a 5 x 6 matrix of diodes whose pitch is 0.018 inches, center to center. While the letters lack much from an artistic viewpoint, they are perfectly legible and lack nothing from an intelligibility standpoint. The selection of a rectangular rather than square matrix is for appearance purposes only. While it is realized that other combinations could be employed to yield more pleasing appearances, it is felt that the 5 x 6 matrix yields a sufficiently pleasing character with a minimum amount of data processing required.

Figure A-8 illustrates the interconnection of the SLP devices to display a single character.

The top row of the recording head will consist of 56 of the character matrices combined into single large matrix of 6 x 280. The row will be physically implemented by wiring together fourteen (14) silicon chips each containing a 6 x 20 integrated SLP array. This necessitates a 0.2 inch spacing between every four (4) characters. The other spacings will be 0.027 inch.

A.2.3 Digital Data

That portion of format not used for alphanumeric characters is organized as a display for 266, eight bit binary words. A silicon light pulser generates each binary bit.

Figure A-9 illustrates the basic building block of the digital data display - an integrated circuit chip containing a 9 x 20 array of SLP diodes. One row and one column of each chip is assigned the function of indexing. This bordering of the bits on each chip will enable easy automatic readout. The remaining columns/chip each represent an eight bit word.

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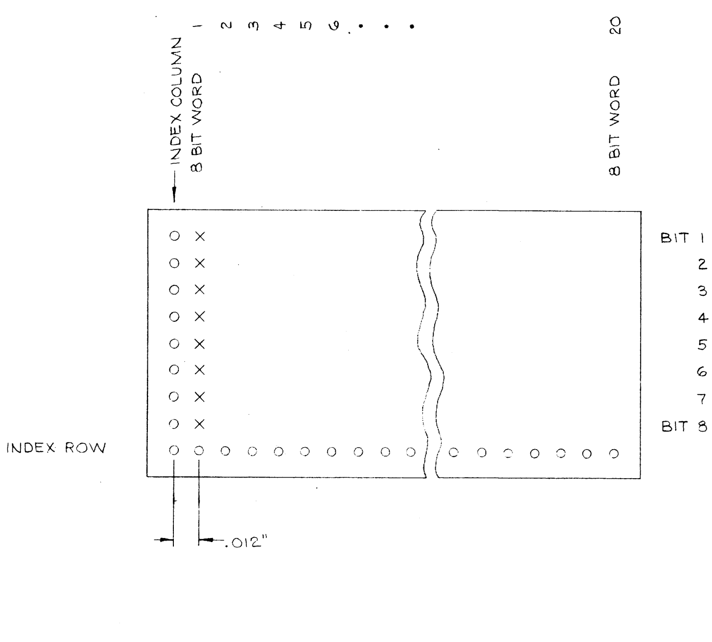

DRAWING NUMBER

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

GENERAL MANUFACTURING INSTRUCTIONS ~~SPI 4.0 ARE PART OF THIS DRAWING.~~
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TOLERANCES: TWO PLACE DEC ± .02, THREE PLACE DEC ± .005, ANGULAR DIM. ± 1°0'

MATERIAL:

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MATLS ______ DATE ______
MFG ______ DATE ______
STDS ______ DATE ______
REL ______ DATE ______
CH DR ______ DATE ______

APPD DATE

APPD DATE

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DWG TITLE FIGURE A-9
9x20 SLP MATRIX CHIP FOR DIGITAL DATA RECORDING

CODE IDENT NO.	SIZE	
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SCALE	WT ACT. CALC LB	SHEET OF

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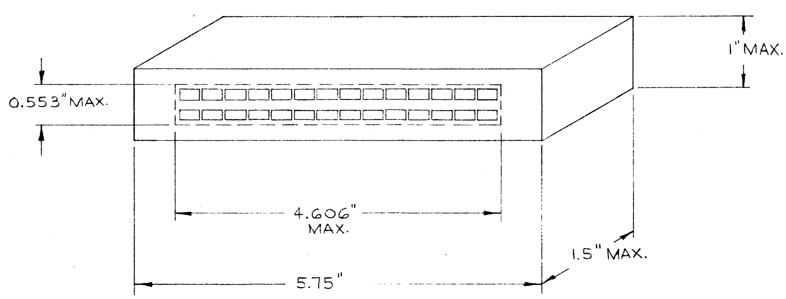

DRAWING NUMBER

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

GENERAL MANUFACTURING INSTRUCTIONS SPI 4.0 ARE PART OF THIS DRAWING. UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. TOLERANCES: TWO PLACE DEC ± .02, THREE PLACE DEC ± .005, ANGULAR DIM. ± 1°0'

MATERIAL:

FINISH:

DR ______ DATE ______
CHK ______ DATE ______
ENG ______ DATE ______
MATLS ______ DATE ______
MFG ______ DATE ______
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REL ______ DATE ______
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DWG TITLE FIGURE A-10 ALPHA NUMERIC RECORD HEAD

CODE IDENT NO.	SIZE	DRAWING NUMBER
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DEFIANCE NO. 1880

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Fourteen of the silicon chips have been placed in the specified format.

Figure A-10 illustrates the solid state record head. The package is compact 1.50 inches wide, 5.75 inches long, and 2.0 inches deep. This package design provides a suitable thermal conductance path away from the light emitting silicon chips, and insures adequate volume for the information of a compact, stress-relieved, output cable from the large number of wires distributed along the edge of the chips.

The chips for both the alpha-numeric data and the digital data are actually identical to economize. Only six rows of the chip are placed in the format area for the former and the entire block is used in the latter. The additional rows could be used to provide 56, eight bit binary words. This would complicate the automatic reader design since these words would not be in the same format as the rest of the binary data.

A.3 DATA PROCESSING

The input data will be supplied by means of 16 parallel input lines. Eight lines specify the alpha-numeric information and the remaining the digital data. Processing of the two types of data will be independent.

As outlined in Section 1.2.3, the recording of alpha-numeric information will be performed by a 5 x 6 matrix of SLP diodes. A conversion from the input code format to a digital code which represents the geometry of the character will be necessary. An analysis of this code reveals that there is no relationship between it and the input code. Therefore, a translation will be required.

In addition to the translation from the input code to SLP code, it will be necessary during the recording sequence to distribute the data bits to the appropriate SLP devices. The establishment of the record sequence will determine the size of the distribution networks.

No conversion is required for the digital data since the recording will be made in the input code format. The data will have to be distributed to the appropriate SLP devices during the record sequence.

A.3.1 Translator

The alphanumeric data is supplied as the American Standard Code for Information Interchange with the addition of an even parity bit. This code represents each alphanumeric character by an eight bit digital word. The SLP code is the thirty bit digital word describing the geometry of the character. Each bit represents a sub-zone or matrix diode. A logical "1" indicates that the particular sub-zone is to be exposed.

There is no mathematical relationship between the input and SLP codes. This leaves only two forms that the translator can take. One is to store a function table of SLP codes with the corresponding ASCI code as the address. The translation from one code to the other is performed by extracting the result from the table as the character is received. The second is to decode each of the characters as it is received and encode a new word as a function of the decode line which has been activated. For the present application, it has been decided to use the latter process. This decision was based upon the relative amount of equipment required.

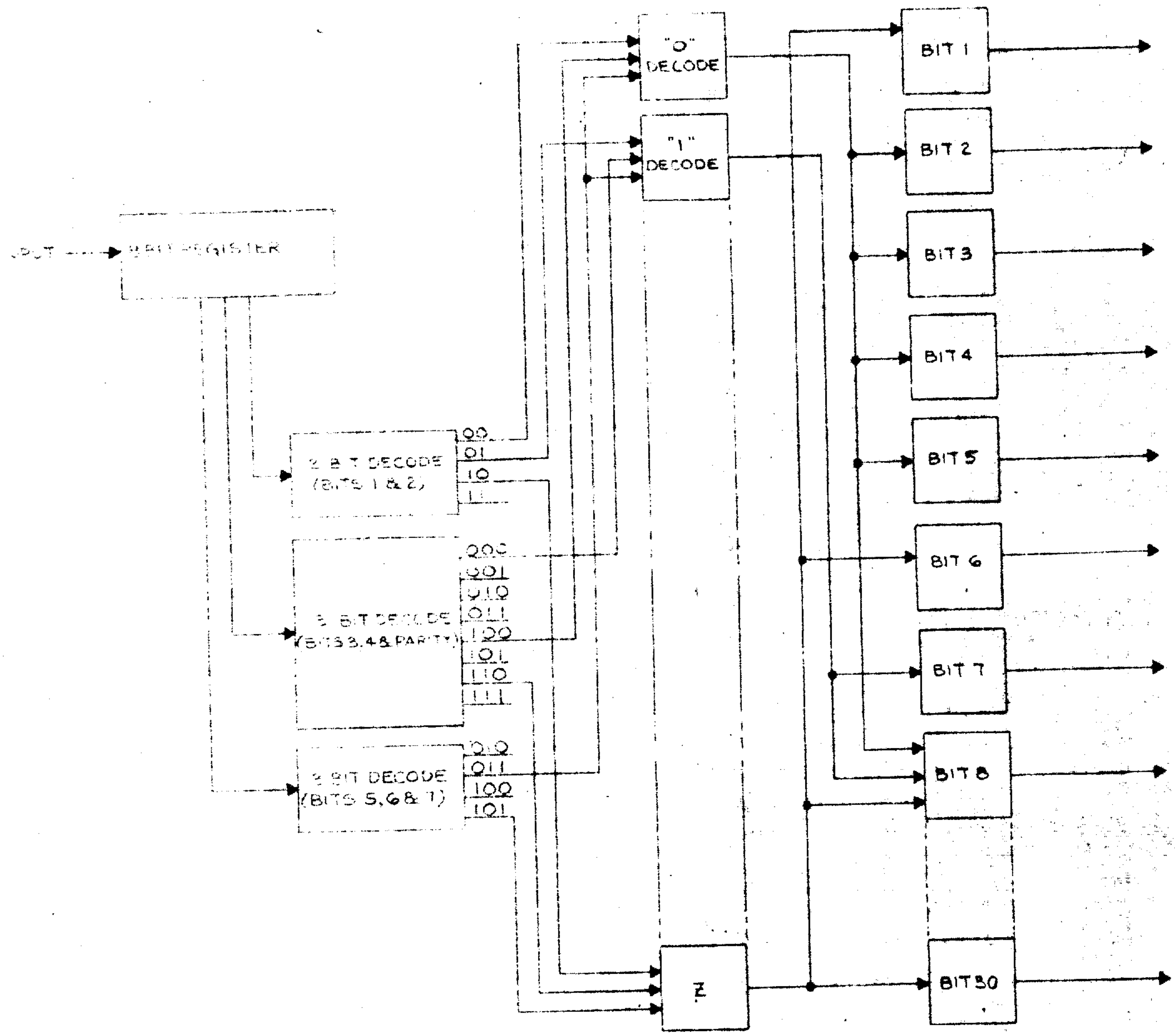

FIGURE A-11. BLOCK DIAGRAM DECODER/ENCODER

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Figure A-11 is a block diagram of the decoder/encoder. As can be seen, the decoder represents a folded matrix and the encoder is merely a series of OR structures, one per bit.

The character information is received and stored in the eight bit flip-flop register. The word is then decoded and under command activates the proper OR structures of the encoder. The encode operation is actually performed in the wiring of the OR structures.

A. 3. 2 Record Sequence

Limitations imposed by the recording head determine the record sequence. These consist of practical restraints on internal wiring of the device.

Column sequential operation over the 15 x 280 array is desirable since it eliminates array distribution hardware. The record time per column is 7 milliseconds and results in a total recording interval of 1. 96 seconds below the allowable 2 seconds.

The problems in wiring within the recording head prevents further division into additional column groups to optimize the economy of the matrix drive circuitry.

The recording sequence will consist of the simultaneous column sequential operation of 15 x 280 array. Data sequences will be supplied to the 15 rows of each array while the appropriate column will be activated in sequence to cover the whole format.

A. 3. 3 Distribution Network

The encoder output supplies the alphanumeric character in

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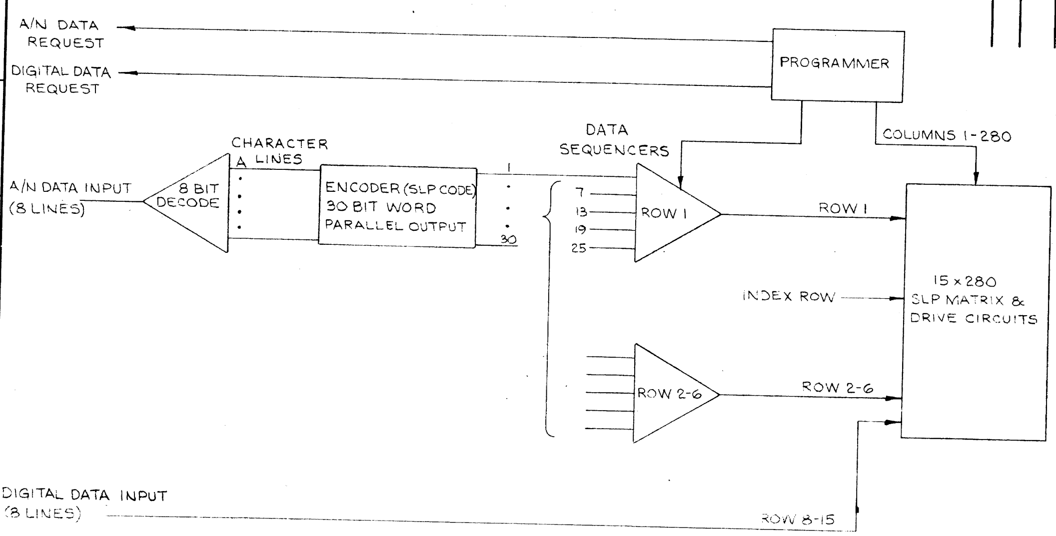

DRAWING NUMBER

GENERAL MANUFACTURING INSTRUCTIONS SPI 4.0 ARE PART OF THIS DRAWING.
UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES.
TOLERANCES: TWO PLACE DEC ± .02, THREE PLACE DEC ± .005, ANGULAR DIM. ± 1°0'

MATERIAL:

FINISH:

NEXT ASSY	USED ON	NEXT ASSY	FINAL ASSY
APPLICATION		QTY REQD	

DR ______ DATE ______
CHK ______ DATE ______
ENG ______ DATE ______
MATLS ______ DATE ______
MFG ______ DATE ______
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REL ______ DATE ______
CH DR ______ DATE ______
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APPD ______ DATE ______

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DWG TITLE FIGURE A-12
BLOCK DIAGRAM
ALPHA/NUMERIC DISPLAY

CODE IDENT NO.	SIZE	DRAWING NUMBER
72314	C	

SCALE | WT ACT. | CALC | LB | SHEET | OF

FCI-10-171 (10-64)
DEFIANCE NO. 1030

parallel form as 30 binary bits. For the record sequence defined in A.3.2, the data is desired in the form of 6 row word sequences consisting of 5 bits. This is achieved by means of a parallel to serial converter. This consists of a two input "AND" gate for each of the 30 bits. The outputs of the "AND" gates are combined in 6 "OR" gates to form the row words. Timing signals from the Programmer are applied to the "AND" gate to assign each of the input bits the proper time slot.

The application of the binary bit to a particular row while at the same time enabling a particular column allocates a unique array element to that bit.

The digital information is available in parallel form from the input buffer register as eight parallel bits. This is suitable for direct application to the SLP matrix for recording. Simultaneous with each shift of data into the register, a different column of the SLP matrix would be enabled assigning a unique SLP to each input data bit.

A.4 SYSTEMS CONFIGURATION

Figure A-12 is a block diagram of the Alphanumeric Record System. Information is received in parallel form into input registers. Under command of the Programmer the alphanumeric data is decoded, encoded in SLP language and by means of parallel to serial converters formed into row word sequences. Upon command each data bit is fed to the proper matrix row, while the proper matrix column is activated to expose the film. The input registers will store the data for the proper duration during the record sequence.